CLAIMS:

We claim:

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1. A method of transferring digital television data in a system having a first frame buffer and a second frame buffer, comprising the steps of:

storing incoming digital television data in the first frame buffer;

reading outgoing digital television data from the second frame buffer;

monitoring refresh of a display device coupled to the system; and

transmitting the outgoing digital television data in the second frame buffer to the display device when a programmed position of the display device is refreshed.

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2. The method of claim 1, further comprising the steps of:

storing the incoming digital television data in the second frame buffer;

reading the outgoing digital television data from the first frame buffer; and

transmitting the outgoing digital television data in the first frame buffer to the display device when the programmed position of the display device is refreshed.

3. The method of claim 1, further comprising the step of:

detecting whether the outgoing digital television data is stored in the first frame buffer or the second frame buffer.

4. The method of claim 1, the monitoring step comprising the step of:

monitoring a horizontal sync and a vertical sync of the display device.

5. The method of claim 1, wherein the outgoing digital television data transmitted to the display device comprises a frame.

6. The method of claim 1, the transmitting step comprising the step of:

transmitting the outgoing digital television data over a peripheral component interconnect (PCI) bus.

7. The method of claim 1, wherein a refresh rate of the incoming digital television data is decoupled from a refresh rate of the outgoing digital television data.

8. A system for transferring digital television data over a local bus, comprising:

a local bus; and

digital television/local bus interface logic coupled to the local bus, comprising:

a digital television interface for receiving incoming digital television data;

a local bus interface for transmitting outgoing digital television data over the local bus;

a first frame buffer for storing the incoming digital television data and the outgoing digital television data in an alternating manner;

a second frame buffer for storing the outgoing digital television data and the incoming digital television data in an alternating manner; and

a memory controller for storing the incoming digital television data to one frame buffer and reading the outgoing digital television data from another frame buffer.

9. The system of claim 8, wherein the local bus comprises a peripheral component interconnect (PCI) bus.

10. The system of claim 8, further comprising:

a display device coupled to the local bus for receiving outgoing digital television data over the local bus.

11. The system of claim 8, wherein the memory controller stores the incoming digital television data to the first frame buffer and reads the outgoing digital television data from the second frame buffer on a first portion of a refresh of a display device and transmits the outgoing digital television data in the second frame buffer to the display device on a second portion of the refresh of the display device.

12. The system of claim 8, wherein the memory controller stores the incoming digital television data to the second frame buffer and reads the outgoing digital television data from the first frame buffer on a first portion of a refresh of a display device and transmits the outgoing digital television data in the first frame buffer to the display device on a second portion of the refresh of the display device.

13. The system of claim 8, wherein the local bus interface monitors a refresh of a display device for receiving the outgoing digital television data.

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14. The system of claim 8, wherein a refresh rate of the incoming digital television data is decoupled from a refresh rate of the outgoing digital television data.

15. The system of claim 8, the digital television/local bus logic further comprising:

a write state machine for detecting whether the incoming digital television data is being written to the first frame buffer or the second frame buffer.

16. The system of claim 8, the digital television/local bus logic further comprising:

a read state machine for informing the memory controller of a frame buffer from which to read the outgoing digital television data.

17. A digital television/local bus interface logic, comprising:

a digital television interface for receiving incoming digital television data;

a local bus interface for transmitting outgoing digital television data;

a first frame buffer for storing the incoming digital television data and the outgoing digital television data in an alternating manner;

a second frame buffer for storing the outgoing digital television data and the incoming digital television data in an alternating manner; and

a memory controller for storing the incoming digital television data to one frame buffer and reading the outgoing digital television data from another frame buffer on a first portion of a refresh of a display device and transmitting the outgoing digital television data in the one frame buffer to the display device on a second portion of the refresh of the display device.

18. The interface logic of claim 17, wherein the local bus interface comprises a peripheral component interconnect (PCI) interface.

19. The interface logic of claim 17, wherein the local bus interface transmits the outgoing digital television data over a local bus.

20. The interface logic of claim 17, wherein the memory controller stores the incoming digital television data to the first frame buffer and reads the outgoing digital television data from the second frame buffer on a first portion of a refresh of the display device and transmits the outgoing digital television data in the second frame buffer to the display device on a second portion of the refresh of the display device.

21. The interface logic of claim 17, wherein the memory controller stores the incoming digital television data to the second frame buffer and reads the outgoing digital television data from the first frame buffer on a first portion of a refresh of the display device and transmits the outgoing digital television data in the first frame buffer to the display device on a second portion of the refresh of the display device.

22. The interface logic of claim 17, wherein a refresh rate of the incoming digital television data is decoupled from a refresh rate of the outgoing digital television data.

23. The interface logic of claim 17, further comprising:

a write state machine for detecting whether the incoming digital television data is being written to the first frame buffer or the second frame buffer.

24. The interface logic of claim 17, further comprising:

a read state machine for informing the memory controller of a frame buffer from which to read the outgoing digital television data.

25. A digital television/local bus interface logic, comprising:

a first interface means for receiving incoming digital television data;

a second interface means for transmitting outgoing digital television data;

a first buffer means for storing the incoming digital television data and the outgoing digital television data in an alternating manner;

a second buffer means for storing the outgoing digital television data and the incoming digital television data in an alternating manner; and

a controller means for storing the incoming digital television data to one buffer means and reading the outgoing digital television data from another buffer means.

26. The interface logic of claim 25, wherein the second interface means for transmitting the outgoing digital television data comprises a peripheral component interconnect (PCI) interface.

27. The interface logic of claim 25, wherein the second interface means for transmitting the outgoing digital television data transmits the outgoing digital television data over a local bus.

28. The interface logic of claim 25, further comprising:

a write state machine means for detecting whether the incoming digital television data is being written to the first frame buffer or the second frame buffer.

29. The interface logic of claim 25, further comprising:

a read state machine means for informing the memory controller of a frame buffer from which to read the outgoing digital television data.

30. The interface logic of claim 25, wherein the first interface means for receiving the incoming digital television data comprises a digital television interface.

31. The interface logic of claim 25, wherein the controller means stores the incoming digital television data to the first storing means and reads the outgoing digital television data from the second storing means on a first portion of a refresh of a display device and transmits the outgoing digital television data in the second storing means to the display device on a second portion of the refresh of the display device.

32. The interface logic of claim 25, wherein the controller means stores the incoming digital television data to the second storing means and reads the outgoing digital television data from the first storing means on a first portion of a refresh of a display device and transmits the outgoing digital television data in the first storing means to the display device on a second portion of the refresh of the display device.

33. The interface logic of claim 25, wherein a refresh rate of the incoming digital television data is decoupled from a refresh rate of the outgoing digital television data.

34. A digital television data handling system, comprising:

a first storing means for storing incoming digital television data and outgoing digital television data in an alternating manner;

a second storing means for storing the incoming digital television data and the outgoing digital television data in an alternating manner;

a monitoring means for monitoring refresh of a display device; and

a transmitting means for transmitting the outgoing digital television data in a storing means to the display device when a programmed position of the display device is refreshed.

35. The system of claim 34, the transmitting means comprising:

a means for reading the outgoing digital television data from a storing means.

36. The system of claim 34, the monitoring means comprising:

a means for monitoring a horizontal sync and a vertical sync of the display device.

37. The system of claim 34, the transmitting means comprising:

a detecting means for detecting whether the outgoing digital television data is stored in the first storing means or the second storing means.

38. The system of claim 34, the transmitting means comprising:

a means for transmitting the outgoing digital television data over a peripheral component interconnect (PCI) bus.

39. The system of claim 34, wherein a refresh rate of the incoming digital television data is decoupled from a refresh rate of the outgoing digital television data.

40. A closed loop digital television data anti-tearing system, comprising:

a local bus;

a graphics controller coupled to the local bus;

a display device for receiving outgoing digital television data from the graphics controller; and

a digital television/local bus interface logic coupled to the local bus for storing incoming digital television data and the outgoing digital television data and selectively providing the outgoing digital television data over the local bus to the graphics controller when a programmed position of the display device is refreshed.

41. The anti-tearing system of claim 40, further comprising:
a core logic coupled between the local bus and the graphics controller.

42. The anti-tearing system of claim 40, further comprising:
a digital television decoder for providing incoming television data to the digital television/local bus interface logic.

43. The anti-tearing system of claim 42, further comprising:
a digital television tuner for providing incoming digital television data to the digital television decoder.

44. The anti-tearing system of claim 40, wherein the graphics controller provides a feedback signal to the digital television/local bus interface logic to indicate whether the programmed position of the display device is refreshed.

45. The anti-tearing system of claim 44, wherein the feedback signal comprises a horizontal sync and a vertical sync of the display device.

46. The anti-tearing system of claim 40, wherein the local bus comprises a peripheral component interconnect (PCI) bus.

47. The anti-tearing system of claim 40, wherein a refresh rate of the incoming digital television data is decoupled from a refresh rate of the outgoing digital television data.

48. A dual stream digital television/local bus interface logic, comprising:
a first digital television interface for receiving a first incoming digital television data stream;
a second digital television interface for receiving a second incoming digital television data stream;

a local bus interface for transmitting a first outgoing digital data stream and a second outgoing digital television data stream;

a first frame buffer for storing the first incoming digital television data stream and the first outgoing digital television data stream in an alternating manner;

a second frame buffer for storing the first outgoing digital television data stream and the first incoming digital television data stream in an alternating manner;

a third frame buffer for storing the second incoming digital television data stream and the second outgoing digital television data stream in an alternating manner;

a fourth frame buffer for storing the second outgoing digital television data stream and the second incoming digital television data stream in an alternating manner; and

a memory controller for storing the first incoming digital television data stream to the first frame buffer or the second frame buffer and reading the first outgoing digital television data stream from the second frame buffer or the first frame buffer on a first portion of a refresh of a display device, storing the second incoming digital television data stream to the third frame buffer or the fourth frame buffer and reading the second outgoing digital television data stream from the fourth frame buffer or the third frame buffer on the first portion of the refresh of the display device, transmitting the first outgoing digital television data stream to the display device on a second portion of the refresh of the display device, and transmitting the second outgoing digital television data stream to the display device on the second portion of the refresh of the display device.

49. The interface logic of claim 48, wherein the local bus interface comprises a peripheral component interconnect (PCI) interface.

50. The interface logic of claim 48, wherein a refresh rate of the first outgoing digital television data stream is decoupled from a refresh rate of the first incoming digital television stream and a refresh rate of the second outgoing digital television data stream is decoupled from the refresh rate of the second incoming digital television data stream.

51. The interface logic of claim 48, further comprising:

a local bus interface buffer for receiving and storing the first outgoing digital television data stream from the first frame buffer and the second frame buffer and for receiving and storing the second outgoing digital television data stream from the third frame buffer and the fourth frame buffer.

52. The interface logic of claim 48, further comprising:

a first set of digital television interface buffers coupled to the first digital television interface for receiving a first incoming digital television data stream; and

a second set of digital television interface buffers coupled to the second digital television interface for receiving the second incoming digital television data stream.

53. A method of transferring digital television data in a computer system, comprising the steps of:

receiving encoded digital television data;

decoding the encoded digital television data to generate decoded digital television data; and

sending the decoded digital television data over a local bus of the computer system to a graphics controller.

54. The method of claim 53, wherein the local bus comprises a peripheral component interconnect (PCI) bus.

55. The method of claim 53, further comprising the step of:

sending the decoded digital television data from the graphics controller to a display device.

56. The method of claim 53, the sending step comprising the step of:

sending decoded digital television data over the local bus to core logic and from the core logic to the graphics controller.

57. A computer system adapted for transferring digital television data, comprising:

a digital television/local bus interface logic for passing decoded digital television data;

a graphics controller for receiving the decoded digital television data over a local bus from the digital television/local bus interface logic; and

a display device for receiving the decoded digital television data from the graphics controller.

58. The computer system of claim 57, wherein the local bus comprises a peripheral component interconnect (PCI) bus.

59. The computer system of claim 57, further comprising:

a core logic for receiving the decoded digital television data from the digital television/local bus interface logic and passing the decoded digital television data to the graphics controller.

60. The computer system of claim 57, further comprising:

a digital television decoder for providing decoded digital television data to the digital television/local bus interface logic.

61. The computer system of claim 60, further comprising:

a digital television tuner for providing encoded digital television data to the digital television decoder.